

# Investigation of High Temperature Process for III-V/SOI Hybrid Photonic Devices with AllInAs Oxidation Current Confinement Layer

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**Abstract**—In order to realize AllInAs oxidation current confinement structures for III-V/SOI hybrid photonic devices, oxidation condition was investigated. With 4-hours ramp up time and 4-hours ramp down time, 63% of PL intensity was maintained even after the oxidation process at 530°C.

## I. INTRODUCTION

THE integration of active optical devices such as light sources and amplifiers on a Si platform is important to realize large scale photonic integrated circuits (PICs)[1]. Our research group proposed to introduce AllInAs oxidation confinement structures in order to achieve efficient current injection in III-V/SOI hybrid active devices [2]. However, typical oxidation temperature is higher than a bonding temperature by plasma activated bonding (PAB). In this paper, we investigated influence of high temperature process to the photoluminescence (PL) of GaInAsP quantum wells (QWs) under various oxidation conditions and wafer structure.

## II. RESULTS

Fig. 1 shows the schematic structure of a sample wafer for this investigation, which composed of a III-V film including a 5-layer GaInAsP MQW(Q1.52) bonded on a SOI substrate by N<sub>2</sub>-PAB(bonding temperature: 150°C[3]). In order to reduce the damage caused by thermal stress occurring at the III-V/Si interface, a GaInAsP/InP superlattice (SL) layer(Q1.20, 7 nm/6 nm × 14 layers) was introduced[4]. In an oxidation process, after preheating an oxidation chamber at 200°C, the chamber was heated up to an oxidation temperature of AllInAs (530°C was applied here), and then, after keeping a desired oxidation time, the chamber was cooled down to 200°C. In this paper, the AllInAs layer was actually not oxidized, (not exposed to the environment) to check only the influence of temperature cycle. As an initial condition for reference, the process was carried out with a wafer not including the SL, under a condition of 10-minutes ramp up time and 1-hour cooling time. As a result, the PL intensity decreased to 18% of the one before the oxidation process (wafer #3 and #4 in Fig. 2). In the experiments, the introduction of the SL and extension of ramp up and ramp down time was tried.

As a result of introducing the SL to a wafer, PL intensity increased by 1.8 times before oxidation (wafer #1 and #3 in Fig. 2). Note that a several-nm shift of peak wavelength was caused through the process. Oxidation processes were carried out to samples with the SL. Fig. 3(a) shows ramp down time dependence of PL intensity when the ramp up time was kept to be 10-minutes, and also Fig. 3(b) shows ramp up time dependence of PL intensity when the ramp down time was kept to be 4 hours. As the result of setting both of ramp up time and ramp down time as 4 hours, the PL intensity of 63% was



Fig. 1. wafer structures for oxidation processes.

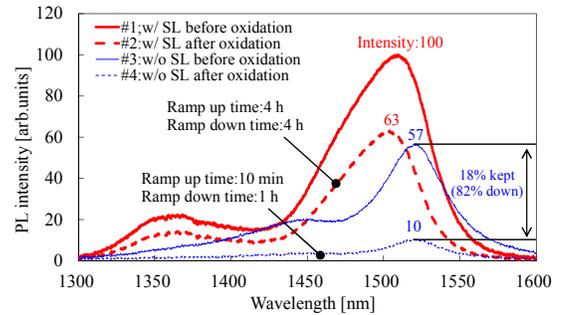


Fig. 2. PL spectra before and after the oxidation process.

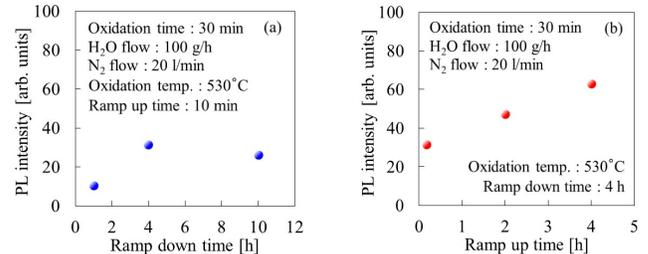


Fig. 3. PL peak intensities as functions of (a) ramp down time and (b) ramp up time maintained compared with one before the oxidation (wafer #1 and #2 in Fig. 2). From these results, we can say avoiding rapid increase and decrease of the chamber temperature is important to maintain the crystal conditions after bonding. From TEM and SIMS measurements, the reason for this tendency may be not only the thermal stress, but some impurity related intermixing. We will investigate the detail in the future.

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