Proceedings of the 16th International Conference on Nanotechnology
Sendai, Japan, August 22-25, 2016

Effect of the HfO_2 passivation on HfS_2 Transistors

T. Kanazawa[1], T. Amemiya[1, 2], *Member IEEE*, V. Upadhyaya[1], A. Ishikawa[3, 2], K. Tsuruta[3], T. Tanaka[2, 1], and Y. Miyamoto[1], *Member, IEEE*
1. Tokyo Institute of Technology, Tokyo, Japan
2. RIKEN, Wako, Japan
3. Okayama University, Okayama, Japan
E mail: kanazawa.t.aa@m.titech.ac.jp

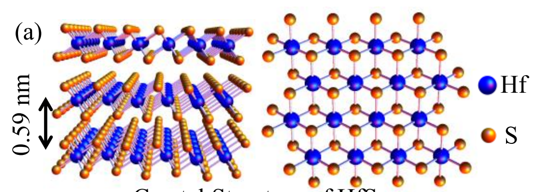
Abstract— **Hafnium Disulfide (HfS_2) is one of the transition metal dichalcogenides which is expected to have high electron mobility and finite bandgap. However, the fabrication process for HfS_2 based electron devices has not been established, and it is required to bring out the superior transport properties of HfS_2. In this report, we have investigated the effects of ALD HfO_2 passivation on the current properties of HfS_2 Transistors. HfO_2 passivation of HfS_2 surface achieved the improvement in drain current and significant reduction of hysteresis. The charge trapping at the outermost surface seems to be the dominant factor for degradation of the current stability.**

I. Introduction

Discovery of the graphene [1] leads the enormous interest in the field of two-dimensional (2D) materials with atomic layer thickness. Graphene shows ultra-high mobility along with other attractive properties and its device applications such as transistors, photodetectors, and gas sensors have been widely studied. However, the absence of bandgap in graphene makes it difficult to suppress the off leakage current of metal-oxide-semiconductor field-effect transistor (MOSFET), which is one of the most important performance parameters for low-power logic applications. Therefore, in recent years, various kind of Transition metal dichalcogenides (TMDs), such as MoS_2 [2], [3] and WSe_2 [4], have been investigated as the post-graphene 2D materials for extremely scaled low-power and high-speed logic applications. These TMDs have both the finite bandgap and extremely thin layer structure (<1 nm), which is attractive for the MOSFETs with the channel length lesser than 10 nm.

Hafnium disulfide (HfS_2) is one of the semiconducting TMDs, which has the 2D crystal structure with octahedral coordination and single layer thickness of 0.6 nm. HfS_2 is expected to have high acoustic phonon limited electron mobility (~1,800 cm^2/Vs) [5] and adequate bandgap (1.2 eV~) [6] as shown in Fig. 1. Previously, we reported the device operation of few-layer HfS_2 MOSFETs with robust current saturation and good on/off ratio [7], [8]. Some other groups also reported the electrical properties of HfS_2 FET from theoretical [9] and experimental [10], [11] approaches. However, the maximum drain current of reported HfS_2 FETs were only several hundreds of nA/μm because the fabrication process for HfS_2 MOSFETs has not been established yet. Additionally, in several cases, large hysteresis and high instability of drain current against measurement sequence were observed due to the charge traps. Moreover, time-dependent degradation of FET current in the atmosphere popped out on continuous evaluation [11], [12]. The atmospheric degradation is one of the critical issues to achieve the high-performance operation of HfS_2 FETs. The degradation seems to be caused by the reaction between HfS_2 surface and moisture, oxygen and other contaminants in the air. To prevent this degradation and instability, the surface of 2D material should be passivated and isolated from the atmosphere to reduce the trap states and absorption of gas atoms, respectively. Previously, the effects of PMMA passivation on HfS_2 FET were observed [12]. Although it indicated some improvement in current performance, the protection using polymer was not beneficial enough to steadily protect the surface from the atmosphere.

In this report, we have investigated the effects of surface passivation by atomic layer deposition (ALD) of HfO_2 dielectric, which is commonly used material as the high-k gate insulator of MOSFETs. The significant reduction in hysteresis was obtained compared to bare devices measured in the atmosphere.



(b) Electrical properties of HfS_2 and typical TMDs

Parameter	Ref.	HfS_2	MoS_2	WSe_2
$\mu_{n,AP}^{\dagger}$ [cm^2/Vs]	[5]	1,833	340	703
m^* [m_0]	[5]	0.24/3.3	0.45	0.33
E_g [eV]	[6]	1.23	1.59	1.32

†acoustic phonon limited electron mobility

Fig. 1 (a) crystal structure and (b) fundamental electrical properties of HfS_2

II. Device Structure and Fabrication

Figure 2 describes the schematic of the fabricated device structure with optical microscope images of the HfS_2 flake after exfoliation and completed device structure, which is covered by HfO_2. HfO_2 cap layer caused a change in the color of flakes. Multi-layer HfS_2 has been used as the channel of the MOSFETs. HfO_2 passivation layer was deposited to

This work was supported by Strategic Information and Communications R&D Promotion Programme (SCOPE) of MIC Japan and JSPS KAKENHI (Grant Number 16H00905).

encapsulate the channel and contacts. Gate bias was applied from the degenerately doped Si substrate as the back gate.

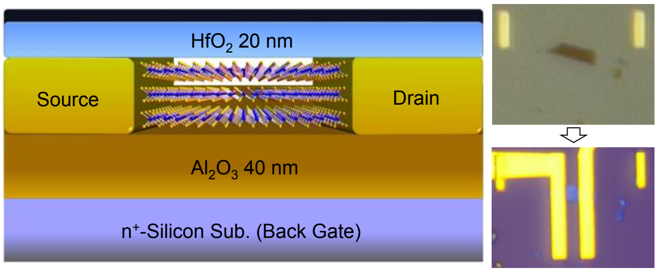


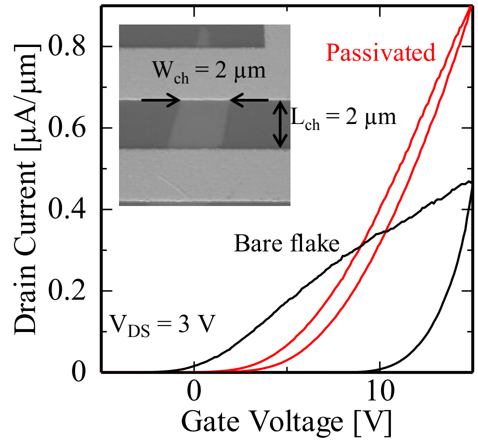
Fig. 2 Schematic device structure and optical images

The fabrication process of MOSFETs based on mechanical exfoliation is as follows. First, the back-gate insulator was formed by the ALD of the 40-nm-thick Al_2O_3 on n^+-Si. Secondly, HfS_2 flakes were transferred to the substrate by the micromechanical exfoliation using polymer adhesive tape with preparing the oxide surface by UV/ozone cleaner. Source/drain (S/D) electrodes and back gate contact were fabricated by the electron beam (EB) lithography and EB evaporation of Ti 20 nm/Au 60 nm and Cr 20 nm/Au 100 nm, respectively. Next, the samples were passivated by HfO_2, which was also deposited by ALD at 150°C using the precursors of Tetrakis(dimethylamino)Hafnium (TDMAH) and H_2O. Then, contact holes to S/D electrodes were formed by CF_4 reactive ion etching of HfO_2. Finally, sample annealing was carried out to improve the HfS_2/HfO_2 interface and contact properties at 250°C in vacuum for 10 min. The fabricated devices were measured by the semiconductor parameter analyzer.

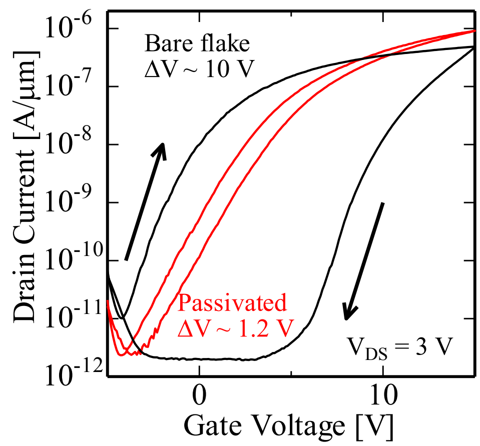
III. Results and Discussions

Figure 3 indicates the transfer characteristics of HfS_2 MOFETs with the similar back gate structure (40-nm-thick Al_2O_3/Si) in (a) linear and (b) semi-log plot. The inset SEM image in (a) is the measured sample as the passivated device. The channel length L_{ch} and width W_{ch} were estimated to be 2 μm. A typical bare HfS_2 sample, which had been exposed to air during the measurement, showed the significant voltage shift ΔV of around 10 V between forward and backward sweep. In contrast, HfO_2 passivated device fabricated in this report showed suppressed ΔV of less than 1.2 V. This improvement in hysteresis by surface passivation suggests that the charge trapping occurred on the outermost surface of HfS_2 flake. The off-leakage current was same for with and without passivation because it was dominated by the gate leakage. The maximum drain current at V_{DS} = 3 V and V_{GS} = 15 V was 0.9 μA/μm for passivated device. Though this value was more than four times higher than previous reports ([8], [10], [11]), the effect of passivation on the drain current is not yet clear due to the process fluctuation. Further investigation and improvement of the S/D contact formation process would achieve the increase of the drain current and clarify the effects of charge trapping on carrier mobility.

Figure 4 shows the output characteristics of the HfO_2 passivated device. Robust current saturation behaviors were observed. The drain current at V_{DS} = 3 V and V_{GS} = 15 V was around 0.8 μA/μm. The difference of current between transfer and output characteristics was around 10%. It was contrary to bare devices, which shows over 80% difference between transfer and output measurement due to the charge trapping degradation. Moreover, the time-dependent degradation of the drain current in the atmosphere was prevented by the HfO_2 capping. Therefore, HfO_2 provides good protection from the oxidation or absorption of any contaminants from the air.



(a) Linear plot



(b) Logarithmic plot

Fig. 3 Comparison of the hysteresis of the transfer curves between bare and HfO_2 passivated HfS_2 MOSFETs.

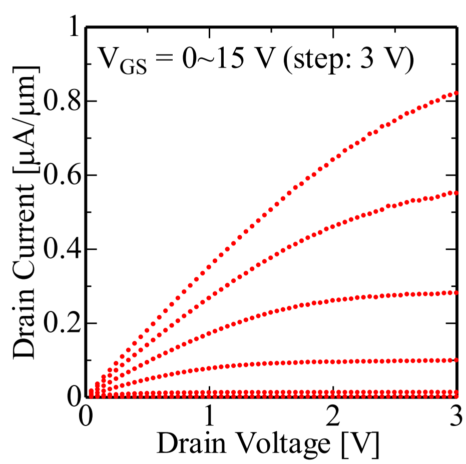


Fig. 4 Output characteristics of HfO_2 passivated MOSFET.

IV. CONCLUSION

In conclusion, we have investigated the effect of surface passivation for HfS_2 MOSFETs using ALD HfO_2, to improve the stability of the I-V characteristics. The maximum drain current of 0.9 μA/μm was observed at $V_{DS} = 3$ V and $V_{GS} = 15$ V. The hysteresis width ΔV were decreased clearly by the passivation from 10 V to 1.2 V. The protection of the surface by the high-k insulator is an efficient way to reduce the trap charges and improve the stability of properties. The reduction of contact resistance is the next measure to achieve the high current operation.

REFERENCES

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, "Electric field effect in atomically thin carbon films." Science, vol.306, pp. 666–669, Oct. 2004.

[2] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kiss, "Single-layer MoS_2 transistors," Nature Nanotech., vol. 6, pp. 217–218, Jan. 2011.

[3] S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Shoi, and K. Kim, "High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals," Nature Comm. Vol. 3, 1011, Aug. 2012.

[4] W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, "Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe_2 Field Effect Transistors," Nano Lett., 2013, vol. 13, pp. 1983–1990. Mar. 2013.

[5] W. Zhang, Z. Huang, W. Zhang, and Y. Li, "Two-dimensional semiconductors with possible high room temperature mobility," Nano Research, vol. 7, pp. 1731–1737, Dec. 2014.

[6] C. Gong, H. Zhang, W. Wang, L. Colombo, R. M. Wallace, and K. Cho, "Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors," Appl. Phys. Lett., vol. 103, 053513, Aug. 2013.

[7] T. Kanazawa, T. Amemiya, A. Ishikawa, K. Tsuruta, T. Tanaka, and Y. Miyamoto "Fabrication of thin-film HfS_2 FET," in Proc. 73rd Device Research Conf., Columbus, OH, June 2015, pp. 217–218.

[8] T. Kanazawa, T. Amemiya, A. Ishikawa, V. Upadhyaya, K. Tsuruta, T. Tanaka, and Y. Miyamoto, "Few-layer HfS_2 transistors," Scientific Reports, vol. 6, 22277, Mar. 2016.

[9] J. Chang, "Modeling of anisotropic two-dimensional materials monolayer HfS_2 and phosphorene metal-oxide semiconductor field effect transistors," J. Appl. Phys., vol. 117, 214502, June 2015.

[10] K. Xu, Z. Wang, F. Wang, Y. Huang, F. Wang, L. Yin, C. Jiang, and J. He, "Ultrasensitive Phototransistors Based on Fe-Layered HfS_2," Advanced Materials, vol. 27, pp. 7781–7887. Oct. 2015.

[11] S. H. Chae, Y. Jin, T. S. Kim, D. S. Chung, H. Na, H. Nam, H. Kim, D. J. Perello, H. Y. Jeong, T. H. Ly, and Y. H. Lee, "Oxidation Effect in Octahedral Hafnium Disulfide Thin Film," ACS Nano, vol. 10 pp. 1309–1316, Jan. 2016.

[12] V. Upadhyaya, T. Kanazawa, and Y. Miyamoto, "Vacuum Annealing and Passivation of HfS_2 FET for Mitigation of Atmospheric Degradation," 2016 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD 2016), A5-7, Hakodate, Japan, July 2016.