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Surface assessment after removing III–V layer on III–V/silicon-on-insulator wafer fabricated by plasma activated bonding

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The partial removal of the III–V layers of a III–V/silicon-on-insulator hybrid wafer was investigated to realize III–V/Si hybrid photonic integrated circuits. Using transmission electron microscopy, we found that an amorphous layer was generated at the interface of a III–V/Si wafer fabricated by N_2-plasma-activated bonding. In order to remove the III–V layers including the amorphous layers without damage to the Si surface, several etching processes were carried out, and the surface conditions were evaluated by X-ray photoelectron spectroscopy. As a result, we demonstrated comparable propagation losses in Si wire waveguides with and without the bonding/removal processes.
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Recently, silicon photonics[1–3] has been an attractive research subject and is a promising material for large-scale photonic integrated circuits (PICs),[4–8] because of its compatibility with CMOS technology and its high refractive-index contrast between Si and SiO_2, allowing for a small waveguide size. However, the realization of highly efficient lasers or optical amplifiers composed only of Si is difficult because of its indirect bandgap. Therefore, III–V/Si hybrid integration by heterogeneous bonding technologies is getting attention as an integration method for optical active devices on silicon-based PICs. Examples include adhesive bonding using the dielectric polymer divinylsiloxane–benzocyclobutene (DVS–BCB)[9–11] and direct bonding with plasma irradiation,[12–15] which does not insert an intermediate layer. Several groups have reported and demonstrated several types of III–V/Si hybrid devices. Our group also proposed N_2-plasma-activated bonding (PAB) and reported a low threshold-current-density III–V/Si hybrid laser.[16] Thus, the field of III–V/Si hybrid integration has grown rapidly.

For fabricating hybrid devices, wafer-level bonding or selective bonding with a small chip (such as a few square centimeters) is usually used. In this case, we have to remove the unwanted III–V-layer regions and expose the Si waveguides to form PICs. However, it was reported that the propagation loss of the Si waveguide after removing the III–V layers in the PICs became higher than before bonding.[17] The increases in scattering and the absorption loss have been considered to be the reasons, although the details have not yet been investigated. In this study, we have investigated the surface conditions after several removal methods and realized a comparable propagation loss for Si waveguides after bonding compared to samples without the bonding process.

The bonding process flow using N_2-PAB is as follows. First, the surfaces of an epitaxially grown InP wafer and a waveguide-patterned silicon-on-insulator (SOI) substrate were cleaned by a typical wet cleaning process and megasonic water cleaning. After the cleaning process, these substrates were loaded into a vacuum chamber and treated by RF plasma irradiation at 500 W for 10 s in a N_2 atmosphere at a chamber pressure of 120 Pa and room temperature. Then, the chamber was maintained at a pressure of 10^{-4} Pa to maintain the activation state of the surface, and the two substrates were temporarily bonded for 180 s at a pressure of 250 kPa.

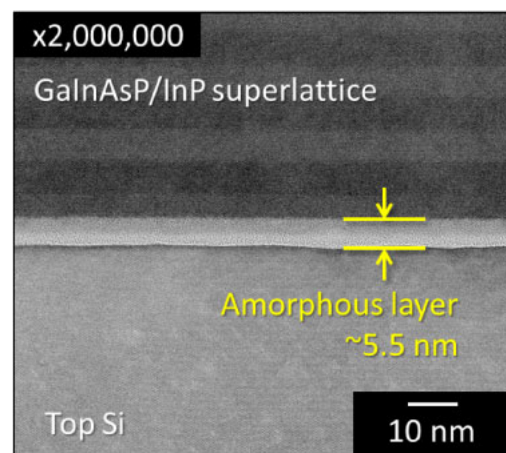

Fig. 1. (Color online) Cross-sectional view of the III–V (upper side)/SOI (lower side) interface fabricated by PAB, as obtained by TEM.

In order to further obtain a strong bond, the two substrates were pressed for 2 h at 250 kPa; meanwhile, the temperature was increased from room temperature to 150 °C. Next, the wafers were released from the pressure, cooled down to room temperature in vacuum for approximately 8 h, and removed from the chamber.

Figure 1 shows a cross-sectional transmission-electron-microscopy (TEM) image of a typical III–V/SOI bonding interface fabricated by PAB. The III–V layers consist of superlattice layers of GaInAsP/InP. An intermediate layer with a thickness of approximately 5.5 nm was observed and considered to be an amorphous layer generated during the PAB process. Similar amorphous layer formation were observed in previous reports.[18,19] This is probably caused by reaction of an activated wafer surface and remaining a little air in the vacuum chamber. According to a secondary-ion mass spectrometry (SIMS) analysis, we have confirmed that this layer contains oxygen, carbon, and hydrogen. Therefore, the formation of the amorphous layer is probably caused by reaction of an activated wafer surface and remaining impurities in the atmosphere even after plasma treatment. We believe this amorphous layer is one of the reason of high transmission loss of the waveguide. In order to expose a flat and clean Si surface, several layer removing process was

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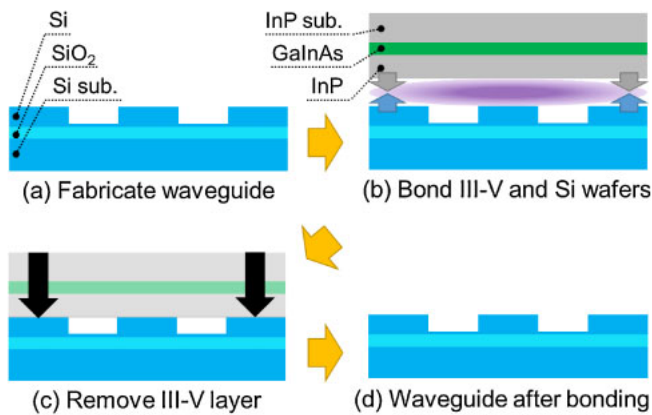

Fig. 2. (Color online) Schematic of the fabrication process.

attempted. At every cleaning step, surface assessment using X-ray photoelectron spectroscopy (XPS) was conducted to identify the most effective process.

Figure 2 shows the schematics of the process flow for surface assessment. On an SOI substrate (thickness: 525 µm) with a 220-nm-thick top-Si layer, a 500-nm-wide and 190-nm-high Si rib waveguide was formed by electron-beam lithography (EBL) and inductively coupled plasma reactive-ion etching (ICP-RIE) using CF_4 gas. The EB resist was Zeon ZEP-520A containing C_{60}, enhancing the dry-etching tolerability, and the JEOL JBX-6300FS EB system operated at a 50-kV acceleration voltage and 100-pA beam current. For easy processing and analysis, a simple III–V wafer structure was adopted in this experiment and compared with full device layer structure we typically used. The simple wafer consisted of a 100-nm-thick undoped GaInAs etching stop layer and 300-nm-thick undoped InP layer epitaxially grown on an InP substrate (thickness: 350 µm). After the SOI and the III–V wafers were bonded by PAB, the InP substrate and GaInAs etching stop layer were selectively etched by HCl and $H_2SO_4 : H_2O_2 : H_2O$ at a ratio of 1 : 1 : 40. Then, four different methods were used to remove the remaining InP layer: wafer (A) used HCl wet etching, wafer (B) used buffered hydrogen fluoride (BHF) wet etching on (A), wafer (C) used CH_4/H_2 dry etching, and wafer (D) used HCl and BHF wet etching on (C). For the waveguide loss measurements, a 1.0-µm-thick SiO_2 cladding was deposited using plasma-enhanced chemical vapor deposition (PECVD) with tetraethyl orthosilicate (TEOS).

Figure 3 shows the microscopic top views of the Si waveguides after HCl wet and CH_4/H_2 dry etching. As shown in sample (A) (Fig. 3, left), the III–V layers appear to be almost completely removed, and the surface was observed to be clean after wet etching compared to the sample (C) (Fig. 3, right). After dry etching, which was not sufficiently cleaned to make low loss waveguides, some contaminants were confirmed. This layer remained due to its low reactivity with CH_4/H_2 gas plasma. High reactivity plasma with an oxide such as CF_4 plasma can etch the layer, but it is not inadvisable because Si surface roughness increases by etching. The appearances of the rest of samples were so similar to the right in Fig. 3.

Figure 4 shows atomic force microscopy (AFM) images of wafer surfaces after removal of the III–V layer using wet or

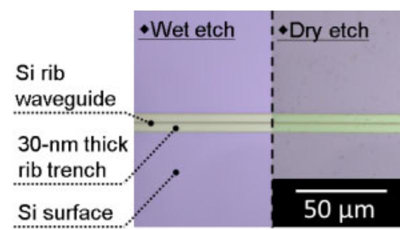

Fig. 3. (Color online) Microscopic top view of a Si waveguide after wet (left) and dry (right) etching.

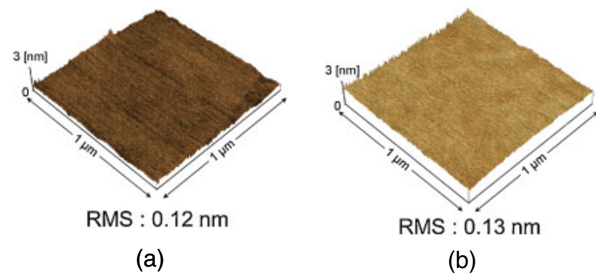

Fig. 4. (Color online) AFM image of a wafer surface after removal of the III–V layer using (a) wet etching and (b) dry etching.

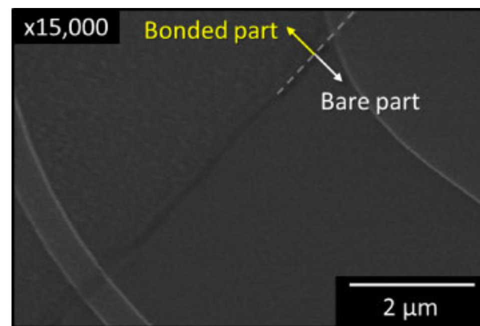

Fig. 5. (Color online) SEM image of the boundary between the bonded and bare parts after dry etching.

dry etching. According to root-mean-square (RMS) values, the values of surface roughness of samples (A) (wet etching) and (C) (dry etching) were measured to be 0.12 and 0.13 nm, respectively, and were not so different. These values are comparable to the surface roughness of a wafer after N_2 plasma treatment for 10 s without bonding.

Figure 5 shows a scanning electron microscopy (SEM) image showing the boundary between the bonded and unbonded regions after dry etching [the same processed sample as wafer (C)]. Compared to the unbonded region, the bonded region was clearly covered with some film with a thickness estimated to be less than a few nanometers. From this, a clean Si surface cannot be exposed by only CH_4/H_2 dry etching. XPS was carried out to further investigate the remaining film after every cleaning process. Table I summarizes the XPS analysis of surfaces of (A) a HCl wet-etched wafer, (B) a HCl and BHF wet-etched wafer, (C) a CH_4/H_2 dry-etched wafer, and (D) a HCl and BHF wet-etched and CH_4/H_2 dry-etched wafer. For reference, (E) a bare SOI substrate was also measured. The SOI substrate was cleaned by H_2SO_4 and BHF. From these measurements, the amount of Si is correlated with the remaining III–V layer thickness,

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Table I. (Color online) XPS measurements (units: at.%).

			Si	O	In	F	N	C	Cu
(A)	Wet etching	HCl	37.4	44.5	0.0	0.4	7.3	10.1	0.3
(B)	Wet etching	HCl + BHF	45.4	37.9	0.0	0.2	0.0	15.9	0.6
(C)	Dry etching	CH_4/H_2	28.6	66.0	1.3	0.0	0.0	3.8	0.3
(D)	Dry etching + Wet etching	CH_4/H_2 + HCl + BHF	46.7	42.9	0.0	0.7	0.0	8.8	0.9
(E)	Reference SOI wafer		68.2	23.1	0.0	0.0	0.0	8.6	0.0

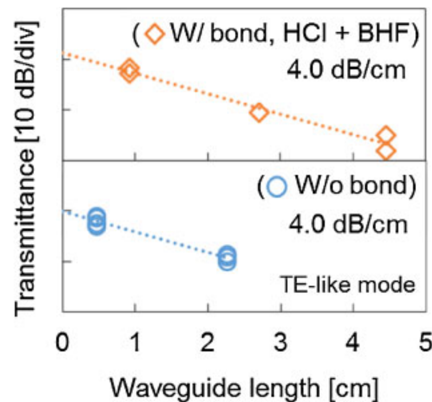

Fig. 6. (Color online) Propagation characteristics.

resulting in wafer (E) having the greatest amount of Si and wafer (C) the least. In contrast, the amount of oxygen indicates the crosscurrent and means that the rest film includes a large amount of oxygen, whose results agreed to the results of SIMS measurement. Indium was detected, and phosphorus was not detected from wafer (C). Further, Indium disappeared after BHF cleaning. Therefore, the amorphous layer was considered to consist of In–O complexes and not pure III–V materials. Owing to XPS, F and N were mainly combined with Si, and C and H were done with C because of the organic chemicals. The detected Cu might originate from the cleaning chemicals. From the above, it was found that HCl and BHF wet-etching was the most effective method and III–V materials remained on the wafer surface by only CH_4/H_2 dry etching.

Transmission measurements using Si wire waveguides were carried out. Figure 6 shows the length dependence of the transmitted light power of the Si waveguides with and without the bonding process. The III–V layer after bonding was etched by (B) HCl and BHF. The other etching methods were not able to remove III–V layer sufficiently, as mentioned above. Therefore, the propagation loss was quite high, and the output power from the Si waveguide was below the measurement limit. As can be observed from the propagation characteristics, the propagation losses were similar for both waveguides, and a low loss of 4 dB/cm was demonstrated.

In conclusion, a Si surface was experimentally evaluated after removing the III–V layer on a III–V/Si wafer fabricated by PAB. In addition, the III–V layer on the III–V/SOI wafer was completely removed by using HCl and BHF wet etching. As a result, a low propagation loss of 4.0 dB/cm was obtained, which is equivalent to the propagation loss of a waveguide without the bonding process. The increase in the propagation loss in Si waveguides on hybrid integration is a major problem; thus, this experiment must contribute the progress of III–V/Si PICs.

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1) Y. A. Vlasov, X.-Z. Bo, J. C. Sturm, and D. J. Norris, Nature **414**, 289 (2001).
2) R. Soref, IEEE J. Sel. Top. Quantum Electron. **12**, 1678 (2006).
3) H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, IEEE J. Sel. Top. Quantum Electron. **12**, 1371 (2006).
4) Y. Vlasov, W. M. J. Green, and F. Xia, Nat. Photonics **2**, 242 (2008).
5) H. Pan, S. Assefa, F. Horst, C. L. Schow, A. V. Rylyakov, W. M. J. Green, M. H. Khater, S. Kamlapurka, C. Reinholm, E. Kiewra, S. M. Shank, C. W. Baks, B. J. Offrein, and Y. A. Vlasov, Proc. 9th Int. Conf. Group IV Photonics, 2012, p. 162.
6) C. R. Doerr, N. K. Fontaine, and L. L. Buhl, IEEE Photonics Technol. Lett. **24**, 697 (2012).
7) Y. Atsumi, M. Oda, J. Kang, N. Nishiyama, and S. Arai, IEICE Trans. Electron. **E95-C**, 229 (2012).
8) Y. Urino, T. Horikawa, T. Nakamura, and Y. Arakawa, Proc. Optical Fiber Communication (OFC) Conf., 2013, OM2J.
9) G. Roelkens, D. Van Thourhout, R. Baets, R. Notzel, and M. Smit, Opt. Express **14**, 8154 (2006).
10) J. Van Campenhout, P. Rojo Romeo, P. Regreny, C. Seassal, D. Van Thourhout, S. Verstuyft, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, and R. Baets, Opt. Express **15**, 6744 (2007).
11) L. Liu, R. Kumar, K. Huybrechts, T. Spuesens, G. Roelkens, E.-J. Geluk, T. de Vries, P. Regreny, D. Van Thourhout, R. Baets, and G. Morthier, Nat. Photonics **4**, 182 (2010).
12) A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, Opt. Express **14**, 9203 (2006).
13) E. Higurashi, T. Imamura, and T. Suga, IEEE Photonics Technol. Lett. **19**, 1994 (2007).
14) X. Sun, A. Zadok, M. J. Shearn, K. A. Diest, A. Ghaffari, H. A. Atwater, A. Scherer, and A. Yariv, Opt. Lett. **34**, 1345 (2009).
15) K. Tanabe, T. Rae, K. Watanabe, and Y. Arakawa, Appl. Phys. Express **6**, 082703 (2013).
16) Y. Hayashi, R. Osabe, K. Fukuda, Y. Atsumi, J. H. Kang, N. Nishiyama, and S. Arai, Jpn. J. Appl. Phys. **52**, 060202 (2013).
17) G. Kurczveil, M. J. R. Heck, J. M. Garcia, H. N. Poulsen, H. Park, D. J. Blumenthal, and J. E. Bowers, Proc. SPIE **7943**, 79430U (2011).
18) A. Fontcuberta i Morral, J. M. Zahler, and H. A Atwater, Appl. Phys. Lett. **83**, 5413 (2003).
19) J. Arokiaraj, S. Tripathy, S. Vicknesh, and A. Ramamz, Electrochem. Solid-State Lett. **8**, G115 (2005).

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